That which is claimed is:

1. A method of forming an electronic device including a substrate and a raised pattern on the substrate, the method comprising:

forming a first insulating layer on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition and forming a second portion of the first insulating layer using a second processing condition;

after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate; and

after removing portions of the first insulating layer, forming a second insulating layer on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer.

2. The method according to Claim 1, wherein the substrate comprises a semiconductor substrate, wherein the raised pattern comprises a trench isolation pattern in the semiconductor substrate, and wherein maintaining portions of the first insulating layer on the substrate comprises maintaining portions of the first insulating layer in trenches defined by the trench isolation pattern.

3. The method according to Claim 1, wherein the substrate comprises an integrated circuit substrate, wherein the raised pattern comprises a pattern of transistor gate electrodes, and wherein maintaining portions of the first insulating layer on the substrate comprises maintaining portions of the first insulating layer between transistor gate electrodes.

4. The method according to Claim 1, wherein the substrate comprises an integrated circuit substrate, wherein the raised pattern comprises a pattern of memory array bit lines, and wherein maintaining

portions of the first insulating layer on the substrate comprises maintaining portions of the first insulating layer between memory array bit lines.

5. The method according to Claim 1, wherein the first insulating layer includes closed voids therein, and wherein removing portions of the first insulating layer comprises opening the voids in the first insulating layer.

6. The method according to Claim 5, wherein openings in the voids are substantially at least as wide as portions of the opened voids between the openings and the substrate.

7. The method according to Claim 5, wherein the closed voids are located in the first insulating layer between portions of the raised pattern.

8. The method according to Claim 5, wherein the second insulating layer fills the opened voids.

9. The method according to Claim 1, wherein:

forming the first portion of the first insulating layer using the first processing condition comprises forming the first portion of the first insulating layer using a first pressure; and

forming the second portion of the first insulating layer using the second processing condition comprises forming the second portion of the first insulating layer using a second pressure different than the first pressure.

10. The method according to Claim 1, wherein:

forming the first portion of the first insulating layer using the first processing condition comprises forming the first portion of the first insulating layer using a first bias power; and

forming the second portion of the first insulating layer using the second processing condition comprises forming the second portion of the

first insulating layer using a second bias power different than the first bias power.

11. The method according to Claim 1, wherein:

forming the first portion of the first insulating layer using the first processing condition comprises forming the first portion of the first insulating layer using a pressure in the range of about 1 milliTorr to about 5 milliTorr and a bias power in the range of about 500 Watts to about 1500 Watts.

12. The method according to Claim 11, wherein forming the first portion of the first insulating layer using the first processing condition comprises using a processing gas including an oxygen gas at a flow rate in the range of about 30sccm to about 150sccm, a helium gas at a flow rate in the range of about 10sccm to about 200sccm, and a silane gas at a flow rate in the range of about 10sccm to about 100sccm.

13. The method according to Claim 1, wherein:

forming the second portion of the first insulating layer using the second processing condition comprises forming the second portion of the first insulating layer using a pressure in the range of about 3 milliTorr to about 10 milliTorr and a bias power in the range of about 1000 Watts to about 5000 Watts.

14. The method according to Claim 13, wherein forming the second portion of the first insulating layer using the second processing condition comprises using a processing gas including an oxygen gas at a flow rate in the range of about 30sccm to about 150sccm, a helium gas at a flow rate in the range of about 10sccm to about 300sccm, and a silane gas at a flow rate in the range of about 10sccm to about 100sccm.

15. The method according to Claim 1, wherein forming the first insulating layer comprises forming the first insulating layer using a high density plasma chemical vapor deposition (HDP-CVD).

16. The method according to Claim 1, wherein removing portions of the first insulating layer comprises etching back portions of the first insulating layer without mechanical polishing while etching back.

17. The method according to Claim 16, wherein removing portions of the first insulating layer further comprises mechanical polishing separate from etching back.

18. The method according to Claim 1, wherein removing portions of the first insulating layer comprises removing portions of the first insulating layer beyond portions of the raised pattern so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed relative to the exposed portions of the raised pattern.

19. The method according to Claim 1, wherein a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern before removing portions of the first insulating layer.

20. A method of forming an electronic device including a substrate and a raised pattern on the substrate, the method comprising:

forming a first insulating layer on the raised pattern and on the substrate wherein a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern;

after forming the first insulating layer, removing portions of the first insulating layer while maintaining portions of the first insulating layer so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed between portions of the raised pattern; and

after removing portions of the first insulating layer, forming a second insulating layer on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer.

21. The method according to Claim 20, wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition including a first pressure and a first bias power and forming a second portion of the first insulating layer using a second processing condition including a second pressure different than the first pressure and a second bias power different than the first bias power.

22. The method according to Claim 20, wherein removing portions of the first insulating layer comprises etching back portions of the first insulating layer without mechanical polishing while etching back.

23. The method according to Claim 20, wherein removing portions of the first insulating layer further comprises mechanical polishing separate from etching back.

24. The method according to Claim 20, wherein the first insulating layer includes closed voids therein, and wherein removing portions of the first insulating layer comprises opening the voids in the first insulating layer.

25. The method according to Claim 24, wherein openings in the voids are substantially at least as wide as portions of the opened voids between the openings and the substrate.

26. The method according to Claim 24, wherein the closed voids are located in the first insulating layer between portions of the raised pattern.

27. The method according to Claim 26, wherein the second insulating layer fills the opened voids.

28. A method of forming an insulation layer in a semiconductor manufacturing process comprising:

forming a first insulation material on a substrate including patterns formed thereon under a first processing condition, wherein the first insulation material has a maximum height and a void having a circular or an elliptical shape formed therein; and

forming a first insulation layer on the substrate including the patterns by forming a second insulation material on the first insulation material under a second processing varied from the first processing condition, wherein the first insulation layer having a level surface covering the patterns includes the voids.

29. The method of claim 28, wherein each of the patterns includes a trench formed in the substrate, a gate structure or a bit line structure formed on the substrate.

30. The method of claim 28, wherein the first insulation material includes a high density plasma (HDP) oxide, and the first insulation layer is formed by a high density plasma chemical vapor deposition (HDP-CVD) process.

31. The method of claim 28, wherein the first processing condition includes a pressure of about 1 to about 5milliTorr and a bias power of about 500 to about 1,500watts.

32. The method of claim 31, wherein the first insulation material is formed using a first processing gas including an oxygen (O_2) gas, a helium (He) gas, and a silane (SiH_4) gas in a flow rate ratio of about 30 to 150; about 10 to about 200: about 10 to about 100.

33. The method of claim 28, wherein the second processing condition includes a second pressure of about 3 to about 10milliTorr and a second bias power of about 1,000 to about 5,000W.

34. The method of claim 33, wherein the second insulation material is formed using a gas including an oxygen gas, a helium gas and a

silane gas, in a flow rate ratio of about 30 to 150; about 10 to about 300: about 10 to about 100.

35. The method of claim 28, wherein the void is positioned over a portion of the substrate between the patterns.

36. The method of claim 28, further comprising etching the first insulation layer by an etch back process to open the void in the first insulation layer and to expose upper faces of the patterns after forming the first insulation layer.

37. The method of claim 36, further comprising forming a second insulation layer that fills up the opened void and covers the patterns after etching the first insulation layer.

38. A method of forming an insulation layer in a semiconductor manufacturing process comprising:

providing a substrate having patterns formed thereon;

forming a first insulation layer that has an level surface and covers the patterns by forming a first insulation material on the substrate, wherein voids are formed at portions of the first insulation layer between the patterns;

forming first insulation layer patterns between the patterns by etching the first insulation layer using an etch back process, wherein the first insulation layer patterns include widely opened voids; and

forming a second insulation layer having a level surface on the first insulation layer patterns by forming a second insulation material, wherein the second insulation layer fills up the opened void and covers the patterns.

39. The method of claim 38, wherein each of the patterns includes a trench formed in the substrate, a gate structure or a bit line structure formed on the substrate.

40. The method of claim 38, wherein the first insulation material

and the second insulation material include HDP oxides, respectively.

41. The method of claim 38, wherein forming the first insulation layer comprises;

forming the first insulation material on the substrate to cover the patterns by an HDP-CVD process under a first processing condition including a first pressure and a first bias power, wherein the first insulation material has a maximum height over the patterns and has voids formed therein; and

forming the first insulation layer having the level surface by forming a second insulation material on the first insulation material using an HDP-CVD process under a second processing condition including a second pressure and a second bias power.

42. The method of claim 41, wherein the first pressure is between about 1 and about 5milliTorr, and the first bias power is between about 500 and about 1,500W.

43. The method of claim 42, wherein the first insulation material is formed using a gas including an oxygen gas, a helium gas, and a silane gas in a flow rate ratio of about 30 to 150: about 10 to about 200: about 10 to about 100.

44. The method of claim 41, wherein the second pressure is between about 3 and about 10milliTorr, and the second bias power is between about 1,000 and about 5,000W.

45. The method of claim 44, wherein the second insulation material is formed using a gas including an oxygen gas, a helium gas and a silane gas in a flow rate ratio of about 30 to 150: about 10 to about 300: about 10 to about 100.

46. The method of claim 38, wherein the voids having circular or elliptical shapes are positioned between the patterns.

47. The method of claim 38, wherein etching the first insulation layer is performed by a wet etch process or a dry etch process.

48. The method of claim 38, wherein the second insulation layer is formed using a second insulation material by an HDP-CVD process under a second processing condition.

49. A method of forming an insulation layer in a semiconductor manufacturing process comprising:

providing a substrate having conductive patterns formed thereon;

forming a first insulation material on the substrate to cover the conductive patterns by an HDP-CVD process under a first processing condition including a first pressure and a first bias power, wherein the first insulation material has a maximum height and has voids formed therein;

forming a first insulation layer having a level surface by forming a second insulation material on the first insulation material under a second processing condition including a second pressure and a second bias power;

forming first insulation layer patterns between the conductive patterns by etching the first insulation layer using an etch back process, wherein the first insulation layer patterns widely open the voids; and

forming a second insulation layer on the first insulation layer patterns by forming a third insulation material, wherein the second insulation layer fills up the opened void and covers the conductive patterns.

50. The method of claim 49, wherein each of the conductive patterns includes a gate structure or a bit line structure formed on the substrate.

51. The method of claim 49, wherein the first insulation material and the second insulation material include HDP oxides.

52. The method of claim 49, wherein the first pressure is between

about 1 and about 5milliTorr, and the first bias power is between about 500 and about 1,500W.

53. The method of claim 49, wherein the first insulation material is formed using a gas including an oxygen gas, a helium gas, and about 10 to about 100sccm by a flow rate of a silane gas in a flow rate ratio of about 30 to 150; about 10 to about 200: about 10 to about 100.

54. The method of claim 49, wherein the second pressure is between about 3 and about 10milliTorr, and the second bias power is between about 1,000 and about 5,000W.

55. The method of claim 49, wherein the second insulation material is formed using a gas including an oxygen gas, a helium gas, and a silane gas in a flow rate ratio of about 30 to 150: about 10 to about 300: about 10 to about 100.

56. The method of claim 49, wherein the voids are positioned between the conductive patterns and the voids have circular or elliptical shapes.

57. The method of claim 49, wherein the etching the first insulation layer is performed by a wet etching process or a dry etching process.

58. The method of claim 49, wherein the second insulation layer is formed using the third insulation material by an HDP-CVD process under a third second processing condition substantially identical to the second processing condition.